WHAT IS CLAIMED IS:

1. A method of processing data comprising:

determining a size of the data to be processed; and

selecting a first processing path if the data size is greater than a first size; and

selecting a second processing path if the data size is less than a first size.

2. The method of Claim 1, wherein the first processing path is used for approximately n-bit data and the second processing path is used for approximately (n/2)-bit data.

3. The method of Claim 2, further comprising operating the first processing path and the second processing path in parallel.

4. The method of Claim 2, further comprising reconfiguring the first processing path to create the second processing path.

5. The method of Claim 4, further comprising:

collecting the processed data from the first processing path and the second processing path at an output; and

selecting the appropriate data to output.

6. A system comprising:

a bus; and

a digital signal processor comprising:

a multiplier having a first structure and a second structure, the first structure processing data up to n-bits and the second structure processing data up to (n/2)-bits; and

a data size selector which configures the multiplier into the first structure when the data is greater than (n/2)-bits and configures the multiplier into the second structure when the data is (n/2)-bits or less.

7. The system of Claim 6, wherein the first structure is a single n-bit multiplier.

8. The system of Claim 6, wherein the second structure includes two (n/2)-bit multipliers.

9. The system of Claim 6, further comprising a plurality of arithmetic logic units to collect the processed data.

10. The system of Claim 6, further comprising a flop which stores the result of the multiplier.

11. The system of Claim 10, further comprising at least one arithmetic logic unit which adds the result from the multiplier to a running total.

12. A method comprising:

determining a size of data to be processed;

configuring a first processing path for data of n-bits if the data size is greater than (n/m)-bits; and

dividing the first processing path into multiple processing paths if the data size is (n/m)-bits or less.

13. The method of Claim 12, further comprising configuring each of the multiple processing paths for data sizes smaller than the first processing path.

14. The method of Claim 12, further comprising dividing the first processing path into m processing paths.

15. The method of Claim 12, further comprising including an n-bit multiplier in the first processing path.

16. The method of Claim 12, further comprising defining m=2.